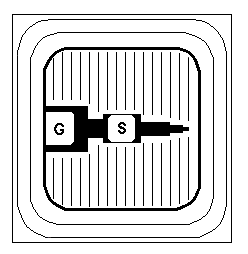
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.043”**

**.041”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential: DRAIN**

**Mask Ref: VF05**

**APPROVED BY: DK DIE SIZE .043” X .041” DATE: 4/27/23**

**MFG: SUPERTEX THICKNESS .011” P/N: VN0545ND**

**DG 10.1.2**

#### Rev B, 7/1